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UTILITY PATENT APPLICATION TRANSMITTAL (Large Entity)

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Docket No.
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TO THE ASSISTANT COMMISSIONER FOR PATENTS

Box Patent Application
Washington, D.C. 20231

Transmitted herewith for filing under 35 U.S.C. 111(a) and 37 C.F.R. 1.53(b) is a new utility patent application invention entitled:

SEMICONDUCTOR DEVICE AND METHOD FOR FABRICATING THE SAME

and invented by:

Yoshihisa NAGANO; Toshie KUTSUNAI; Yuji JUDAI; Yasuhiro UEMOTO; Eiji FUJII

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Enclosed are:

Application Elements

1. ☒ Filing fee as calculated and transmitted as described below
2. ☒ Specification having 43 pages and including the following:
 - a. ☒ Descriptive Title of the Invention
 - b. ☐ Cross References to Related Applications (if applicable)
 - c. ☐ Statement Regarding Federally-sponsored Research/Development (if applicable)
 - d. ☐ Reference to Microfiche Appendix (if applicable)
 - e. ☒ Background of the Invention
 - f. ☒ Brief Summary of the Invention
 - g. ☒ Brief Description of the Drawings (if drawings filed)
 - h. ☒ Detailed Description
 - i. ☒ Claim(s) as Classified Below
 - j. ☒ Abstract of the Disclosure

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Application Elements (Continued)

3. ☒ Drawing(s) *(when necessary as prescribed by 35 USC 113)*
- a. ☒ Formal Number of Sheets 11
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- a. ☒ Newly executed *(original or copy)* ☐ Unexecuted
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Signed statement attached deleting inventor(s) named in the prior application,
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The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under
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6. ☐ Computer Program in Microfiche *(Appendix)*
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Accompanying Application Parts

8. ☒ Assignment Papers *(cover sheet & document(s))*
9. ☐ 37 CFR 3.73(B) Statement *(when there is an assignee)*
10. ☐ English Translation Document *(if applicable)*
11. ☐ Information Disclosure Statement/PTO-1449 ☐ Copies of IDS Citations
12. ☐ Preliminary Amendment
13. ☒ Acknowledgment postcard
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15. ☒ Certified Copy of Priority Document(s) *(if foreign priority is claimed)*

16. ☒ Additional Enclosures *(please identify below):*

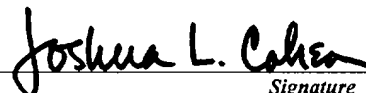
Associate Power of Attorney (2 pages)
Claim to Right of Priority

Fee Calculation and Transmittal

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For	#Filed	#Allowed	#Extra	Rate	Fee
Total Claims	27	- 20 =	7	x \$22.00	\$154.00
Indep. Claims	2	- 3 =	0	x \$82.00	\$0.00
Multiple Dependent Claims (check if applicable) <input type="checkbox"/>					\$0.00
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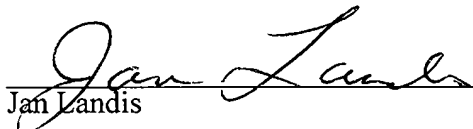
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New Utility Transmittal (in duplicate)
Associate Power of Attorney (2 pages)
Specification and Claims (43 pages)
DEC/POA (3 pages)
(11) Sheets of Formal Drawings
Claim to Right of Priority (w/1 priority document attached)
PTO-1595
Assignment Document (3 pages)
(2) checks

BACKGROUND OF THE INVENTION

1. FIELD OF THE INVENTION:

5 The present invention relates to a semiconductor device including a capacitor having a dielectric film formed of a dielectric material having a high dielectric constant or a ferroelectric material, and a method for fabricating the same.

10 2. DESCRIPTION OF THE RELATED ART:

15 Recently, as functions of consumer electric and electronic appliances have been more and more advanced along with higher processing rates and lower power consumption of microcomputers, the size of semiconductor devices used in the microcomputers has rapidly decreased. This has been accompanied by the serious problem of unnecessary radiation, which is electromagnetic wave noise generated from the electric and electronic appliances.

20 In order to reduce the unnecessary radiation, technologies for incorporating a capacitor having a large capacitance including a dielectric film formed of a dielectric material having a high dielectric constant (hereinafter, referred to as a "high dielectric constant material film") into a semiconductor device have been the target of attention. Furthermore, in accompaniment of higher integration dynamic RAMs (DRAMs), technologies for using a high dielectric constant material film in the capacitor, in lieu of a silicon oxide film and a silicon nitride film which are conventionally used, have been widely studied.

Furthermore, in order to realize non-volatile RAMs which are operable at lower voltages and provide higher read/write rates, ferroelectric material films exhibiting spontaneous polarization have been actively
5 studied.

The most important point in realizing semiconductor devices having the above-described features is to develop a structure which permits multi-layered intercon-
10 nects without deteriorating the characteristics of the capacitor and a method for fabricating such a structure.

Hereinafter, an exemplary conventional method for fabricating a semiconductor device 500 will be described
15 with reference to Figures 10A through 10E (cross-sectional views).

As shown in Figure 10A, an integrated circuit 4 and a device isolating insulating layer 5 are formed on
20 a supporting substrate 1. The integrated circuit 4 includes a MOS field effect transistor (MOSFET) having a gate electrode 2, and source and drain regions 3. An insulating layer 6 is formed on the resultant laminate. A film which will act as a lower electrode 7 of a capaci-
25 tor 10 is formed on the insulating layer 6 by sputtering or electron beam deposition. Then, a dielectric film 8 made of a high dielectric constant material film or a ferroelectric material film is formed on the film to act as the lower electrode 7 by metal organic deposition,
30 metal organic chemical vapor deposition, or sputtering. Subsequently, a film which will act as an upper electrode 9 is formed on the dielectric film 8 by sputtering or electron beam deposition. Then, the layers 7, 8 and 9

are patterned into desirable patterns, thereby forming a capacitor 10.

5 Next, as shown in Figure 10B, a first interlayer
insulating film 11 is formed on the insulating layer 6 so
as to cover the capacitor 10. Contact holes 12 are formed
so as to run through the first interlayer insulating film
11 and reach, respectively, the lower electrode 7 and the
upper electrode 9 of the capacitor 10. Contact holes 13
10 are also formed so as to run through the first interlayer
insulating film 11 and the insulating layer 6 and reach,
respectively, the source and drain regions 3. Conductive
layers are formed on the first interlayer insulating film
11 and in the contact holes 12 and 13 by sputtering or
15 the like, and patterned into desired patterns. Thus,
first interconnects 14 for electrically connecting the
integrated circuit 4 and the capacitor 10 are formed.
The first interconnects 14 are then subjected to a
thermal treatment.

20 As shown in Figure 10C, a second interlayer
insulating film 15 are formed on the resultant laminate
so as to cover the first interconnects 14. The second
interlayer insulating film 15 is formed by substantially
25 planarizing, by etch-back, a silicon oxide film formed by
plasma CVD using tetraethyl orthosilicate (TEOS) (herein-
after, referred to as a "plasma TEOS film") or a laminate
including the above-described plasma TEOS film and a
silicon-on-glass (SOG) film.

30 As shown in Figure 10D, contact holes 16 are
formed so as to run through the second interlayer insu-
lating film 15 and reach the first interconnects 14.

Second interconnects 17 are selectively formed on the second interlayer insulating film 15 and in the contact holes 16 so as to be electrically connected to the first interconnects 14. The second interconnects 17 are then subjected to a thermal treatment.

As shown in Figure 10E, a passivation layer 18 is formed so as to cover the second interconnects 17 on the resultant laminate. Thus, the semiconductor device 500 is fabricated.

In the above-described method for fabricating the semiconductor device 500, the second interlayer insulating film 15 needs to be formed so as to have no step and a flat top surface and thus have a sufficient step coverage property. The reason for this is that, when the second interlayer insulating film 15 has a step, the second interconnects 17 to be formed thereon may disadvantageously be disconnected at the step. Accordingly, the conventional second interlayer insulating film 15 formed of a plasma TEOS film or the like needs to have a thickness h_1 (Figure 10C) of about 1 μm or more on the first interconnects 14 above the upper electrode 9 and also have a thickness h_2 (Figure 10C) of about 2 μm or more on the first interlayer insulating film 11 on an edge of the dielectric film 8 formed of a high dielectric constant material film or a ferroelectric material film.

Generally, however, when the force per unit thickness is constant, a thicker layer results in a stronger tensile or compressive stress. Thus, when the thickness of the second interlayer insulating film 15 is as thick as above-described, a significantly strong

stress is applied to the capacitor 10 provided below the second interlayer insulating film 15.

Specifically when the second interlayer insulating film 15 is formed of a plasma TEOS film, the compressive stress acting on the dielectric film 8 prevents the polarization of the dielectric material forming the dielectric film 8. As a result, the physical properties of the dielectric film 8 formed of the high dielectric constant material or ferroelectric material deteriorate.

As used herein, the term "stress" refers to a force for contracting the layer (hereinafter, referred to as a "tensile stress") and/or a force for expanding the layer (hereinafter, referred to as a "compressive stress").

SUMMARY OF THE INVENTION

A semiconductor device of the present invention includes: a capacitor provided on a supporting substrate having an integrated circuit thereon and including a lower electrode, a dielectric film, and an upper electrode; a first interlayer insulating film provided so as to cover the capacitor; a first interconnect selectively provided on the first interlayer insulating film and electrically connected to the integrated circuit and the capacitor through a first contact hole formed in the first interlayer insulating film; a second interlayer insulating film formed of ozone TEOS and provided so as to cover the first interconnect; a second interconnect selectively provided on the second interlayer insulating film and electrically connected to the first interconnect

through a second contact hole formed in the second interlayer insulating film; and a passivation layer provided so as to cover the second interconnect.

5 In one embodiment, the dielectric film is formed from either a dielectric material having a high dielectric constant or a ferroelectric material.

10 In one embodiment, the second interconnect is provided on the second interlayer insulating film so as to cover at least a part of the capacitor.

15 The passivation layer may be formed of a laminate including a silicon oxide film and a silicon nitride film.

20 In one embodiment, a hydrogen supplying layer is further provided between the first interconnect and the second interlayer insulating film excluding an area in which the capacitor is provided.

25 The first interconnect may be formed from a laminate including titanium, titanium nitride, aluminum and titanium nitride; a laminate including titanium, titanium nitride and aluminum; a laminate including titanium, titanium tungsten, aluminum and titanium tungsten; or a laminate including titanium, titanium tungsten and aluminum.

30 Preferably, a Si-OH bond absorption coefficient of the second interlayer insulating film at a wavelength corresponding to 3450 cm^{-1} is 800 cm^{-1} or less.

Preferably, the second interlayer insulating film has a tensile stress of 1×10^7 dyn/cm² to 3×10^9 dyn/cm² inclusive.

5 Preferably, the second interlayer insulating film has a thickness of 0.3 μ m to 1 μ m inclusive.

10 The second interconnect may be formed from a laminate including titanium, aluminum and titanium nitride; a laminate including titanium and aluminum; or a laminate including titanium, aluminum and titanium tungsten.

15 A method for fabricating a semiconductor device of the present invention includes the steps of: sequentially forming a lower electrode, a dielectric film, and an upper electrode on a supporting substrate having an integrated circuit, thereby forming a capacitor; forming a first interlayer insulating film so as to cover the capacitor; forming a first contact hole in the first interlayer insulating film; selectively forming a first interconnect in the first contact hole and on a prescribed area of the first interlayer insulating film so as to be electrically connected to the integrated circuit and the capacitor; forming a second interlayer insulating film of ozone TEOS so as to cover the first interconnect; subjecting the second interconnect to a first thermal treatment; forming a second contact hole in the second interlayer insulating film; selectively forming a second interconnect in the second contact hole and on a prescribed area of the second interlayer insulating film so as to be electrically connected to the first interconnect; subjecting the second interconnect to a second

thermal treatment; and forming a passivation layer so as to cover the second interconnect.

5 In one embodiment, the dielectric film is formed from either a dielectric material having a high dielectric constant or a ferroelectric material.

10 In one embodiment, the method further includes the step of etching back the second interlayer insulating film using the second interconnect as a mask to such an extent as to almost expose the first interconnect.

15 In one embodiment, the step of forming the second interconnect includes the step of forming the second interconnect so as to cover at least a part of the capacitor.

20 In one embodiment, the passivation layer is formed of a laminate including a silicon oxide film and a silicon nitride film, and the silicon oxide film is formed by normal-pressure CVD, low-pressure CVD or plasma CVD, with using silane, disilane or ozone TEOS, so as to have a tensile stress.

25 In one embodiment, the method further includes the steps of: after the first interconnect is formed, forming a hydrogen supplying layer on the first interconnect excluding an area where the capacitor is provided; and performing a third thermal treatment.

30 The hydrogen supplying layer may be formed from either silicon nitride or silicon nitride oxide by plasma CVD.

Preferably, the third treatment performed after the formation of hydrogen supplying layer is performed at a temperature in the range of 300°C to 450°C inclusive.

5 Preferably, the third treatment performed after the formation of the hydrogen supplying layer is performed in an oxygen atmosphere, a nitrogen atmosphere, an argon atmosphere, or an atmosphere of a mixed gas thereof.

10

The first interlayer insulating film may be formed of silicon oxide by normal-pressure CVD or low-pressure CVD, with using silane, disilane or ozone TEOS.

15

The first interlayer insulating film may be formed of phosphorus-doped silicon oxide by normal-pressure CVD or low-pressure CVD.

20

Preferably, an ozone concentration upon forming the second interlayer insulating film using ozone TEOS is set to be 5.5% or more.

25

Preferably, the second interlayer insulating film after being subjected with the first thermal treatment has a tensile stress of 1×10^7 dyn/cm² to 2×10^9 dyn/cm² inclusive.

30

Preferably, the first thermal treatment is performed at a temperature in the range of 300°C to 450°C inclusive.

Preferably, the first thermal treatment is performed in an atmosphere containing at least oxygen.

Preferably, the second thermal treatment is performed at a temperature in the range of 300°C to 450°C inclusive.

5 Preferably, the second thermal treatment is performed in an atmosphere containing at least one of nitrogen, argon and helium.

10 According to the present invention, the second interlayer insulating film is formed of an ozone TEOS film, which performs self-reflow when being formed. Therefore, sufficient step coverage is obtained as a result of sufficient planarization of a top surface of the second interlayer insulating film without increasing
15 the thickness of an area of the second interlayer insulating film above a capacitor (i.e., without generating any step). Specifically, the thickness of the second interlayer insulating film is about 1 μm or less. Since the second interlayer insulating film to be formed is
20 thin, the stress acting on the capacitor is alleviated.

 Since the ozone TEOS film has a tensile stress, the deterioration in the characteristics of the capacitor caused by the stress is suppressed.

25 When the second interconnect is formed on the second interlayer insulating film so as to cover at least a part of the capacitor, the stress acting on the capacitor by the passivation layer is counteracted by the
30 stress in the second interconnect provided on the capacitor. Accordingly, the stress acting on the capacitor is alleviated.

When the passivation layer is formed of a laminate including a silicon oxide film and a silicon nitride film, the silicon oxide film is a tensile stress. Thus, by forming a silicon nitride film having a large compressive stress by plasma CVD on the passivation layer, the stress in the passivation layer is counteracted. As a result, the stress acting on the capacitor is alleviated.

When a hydrogen supplying layer is provided, the hydrogen in the hydrogen supplying layer is thermally diffused to a supporting substrate having a semiconductor integrated circuit formed thereon by annealing the hydrogen supplying layer. Thus, the supporting substrate recovers from the damage caused during fabrication of the integrated circuit. The hydrogen supplying layer can be formed of a silicon nitride or a silicon nitride oxide containing a sufficient amount of hydrogen therein. By performing the above-mentioned annealing (thermal treatment) in an oxygen atmosphere, a nitrogen atmosphere, an argon atmosphere or a mixture of the above gases after the hydrogen supplying layer is formed, thermal diffusion of hydrogen is performed smoothly.

When the first interconnect and/or the second interconnect is formed of the above-mentioned laminate, a highly reliable interconnect is obtained without causing penetration of the constituent material.

When the ozone TEOS film forming the second interlayer insulating film has a Si-OH bond absorption coefficient of 800 cm^{-1} or less at a wavelength corresponding to 3450 cm^{-1} , the moisture content in the ozone TEOS film is at a minimum possible value. Accordingly,

moisture which deteriorates the characteristics of the capacitor, especially OH radicals and H radicals, is restricted from entering the capacitor.

5 When the ozone TEOS film forming the second interlayer insulating film has a tensile stress of 1×10^7 dyn/cm² to 3×10^9 dyn/cm² inclusive, adverse effects on the capacitor (e.g., undesirable restriction of polarization) caused by the stress applied to the capacitor are alleviated. Thus, the characteristics of the capacitor are improved. This effect largely relies on the fact that the stress is a tensile stress. A capacitor which is supplied with a tensile stress, e.g., from an ozone TEOS film has more preferable characteristics than a capacitor which is supplied with a compressive stress, e.g., from a plasma TEOS film, even when the absolute values of the stresses are equal.

20 By reducing the thickness of the ozone TEOS film forming the second interlayer insulating film to a range of 0.3 μ m to 1 μ m inclusive, the stress in the ozone TEOS film is lowered, and the stress acting on the capacitor from the ozone TEOS film is also lowered. Accordingly, the characteristics of the capacitor are improved.

25 Furthermore, when the second interlayer insulating film is etched back using the second interconnect as a mask, the thickness of an area of the second interlayer insulating film above the capacitor (where the second interconnect is not usually provided) is further reduced

30 (e.g., to 0.5 μ m or less). Thus, the effect of reducing the stress and suppressing the deterioration in the characteristics are further enhanced.

When the ozone concentration upon forming the ozone TEOS film as the second interlayer insulating film is 5.5% or more, the stress in the ozone TEOS film is alleviated. The moisture content in the ozone TEOS film is also reduced. Moreover, generation of cracks by thermal treatment is prevented. Accordingly, the characteristics of the capacitor are further improved.

When the first interlayer insulating film is formed of a silicon oxide film by normal-pressure CVD or low-pressure CVD using silane, disilane or ozone TEOS, or formed of a phosphorus-doped silicon oxide film by normal-pressure CVD or low-pressure CVD, the resultant layer is reliable.

When the temperature for the thermal treatment (first thermal treatment) performed on the second interlayer insulating film (the ozone TEOS film) is in the range of 300°C to 450°C inclusive, the ozone TEOS film becomes dense. When the above-described thermal treatment is performed in an atmosphere containing oxygen, oxygen is supplied to the dielectric film. Thus, the characteristics of the capacitor are improved.

When the thermal treatment on the second interconnect (i.e., the second thermal treatment) is performed under the above-described conditions, the second interconnect becomes dense, and the stress acting on the capacitor is lowered.

Thus, the invention described herein makes possible the advantages of providing a semiconductor device having a structure for allowing a capacitor

thereof to have superior characteristics as a result of suppressing deterioration in the characteristics caused by a stress applied on the capacitor, and a method for fabricating such a semiconductor device.

5

These and other advantages of the present invention will become apparent to those skilled in the art upon reading and understanding the following detailed description with reference to the accompanying figures.

10

BRIEF DESCRIPTION OF THE DRAWINGS

Figures 1A through 1E are cross-sectional views illustrating a method for producing a semiconductor device according to a first example of the present invention;

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Figure 2 is a cross-sectional view of a semiconductor device in a modification of the first example according to the present invention;

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Figure 3 is a graph illustrating characteristics of a capacitor in the semiconductor device in the first example;

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Figures 4A through 4E are cross-sectional views illustrating a method for producing a semiconductor device according to a second example of the present invention;

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Figure 5 is a graph illustrating characteristics of a capacitor in the semiconductor device in the second example;

Figures 6A through 6E are cross-sectional views illustrating a method for producing a semiconductor device according to a third example of the present invention;

5

Figure 7 is a graph illustrating characteristics of a capacitor in the semiconductor device in the third example;

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Figure 8A is a partial plan view of the semiconductor device according to the third example of the present invention;

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Figures 8B and 8C are modified plan views of semiconductor devices of the third example;

20

Figure 9 is a graph illustrating characteristics of a capacitor in the semiconductor device in the third example;

25

Figures 10A through 10E are cross-sectional views illustrating a conventional method for producing a semiconductor device;

30

Figure 11A is a schematic cross-sectional view of a silicon oxide film formed by conventional plasma CVD so as to cover a wiring pattern provided on a substrate surface; and

Figure 11B is a schematic cross-sectional view of a silicon oxide film formed by thermal CVD performed in an atmosphere containing ozone so as to cover a wiring pattern provided on a substrate surface.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

The present invention will be described by way of illustrative but not limiting examples with reference to the accompanying drawings. Identical or similar elements described with reference to Figures 10A through 10E will bear identical reference numerals therewith and detailed descriptions thereof will be omitted.

(Example 1)

Figures 1A through 1E are cross-sectional views illustrating a method for fabricating a semiconductor device 100 according to a first example of the present invention.

As shown in Figure 1A, an integrated circuit 4 and a device isolating insulating layer 5 are formed on a supporting substrate 1 formed of silicon or the like. The integrated circuit 4 includes a MOSFET having a gate electrode 2, and source and drain regions 3. An insulating layer 6 is formed on the resultant laminate. A film which will act as a lower electrode 7 of a capacitor 10 is formed on the insulating layer 6 by sputtering or electron beam deposition. Then, a dielectric film 8 made of a high dielectric constant material film or a ferroelectric material film is formed on the film to act as the lower electrode 7 by metal organic deposition, metal organic chemical vapor deposition, or sputtering. Subsequently, a film which will act as an upper electrode 9 is formed on the dielectric film 8 by sputtering or electron beam deposition. Then, the layers 7, 8 and 9 are patterned into desirable patterns, thereby forming a capacitor 10.

The formation of the insulating layer 6 can be omitted, in which case the capacitor 10 is formed directly on the device isolating insulating layer 5. This is also applicable to examples described below.

5

The lower electrode 7 and the upper electrode 9 of the capacitor 10 can be formed of, for example, platinum, palladium, ruthenium, ruthenium oxide, iridium, or iridium oxide. In the case where the dielectric film 8 is formed of a high dielectric constant material, a material having a specific dielectric constant of 20 to 500 inclusive can be used. Alternatively, in the case where the dielectric film 8 is formed of a ferroelectric material, a material having remnant polarization without any need of application of an external voltage can be used. Examples of the high dielectric constant materials and ferroelectric materials usable for the dielectric film 8 include $\text{Ba}_{1-x}\text{Sr}_x\text{TiO}_3$, SrTiO_3 , Ta_2O_5 , $\text{PbZr}_{1-x}\text{Ti}_x\text{O}_3$, $\text{SrBi}_2\text{Ta}_2\text{O}_9$, and $\text{SrBi}_2\text{Ta}_x\text{Nb}_{1-x}\text{O}_9$.

10

15

20

Next, as shown in Figure 1B, a first interlayer insulating film 111 is formed on the insulating layer 6 so as to cover the capacitor 10. The first interlayer insulating film 111 is formed of a silicon oxide film, which is produced by thermal CVD using, as a material gas, gas-state TEOS in a normal-pressure atmosphere containing ozone (hereinafter, such a silicon oxide film will be referred to as an "ozone TEOS film"). Contact holes 12 are formed so as to run through the first interlayer insulating film 111 and reach, respectively, the lower electrode 7 and the upper electrode 9 of the capacitor 10. Contact holes 13 are also formed so as to run through the first interlayer insulating film 111 and

25

30

the insulating layer 6 and reach, respectively, the source and drain regions 3. A laminate including titanium, titanium nitride, aluminum and titanium nitride is formed on the first interlayer insulating film 111 and in the contact holes 12 and 13 by sputtering or the like, and then patterned into desired patterns. Thus, first interconnects 14 for electrically connecting the integrated circuit 4 and the capacitor 10 are formed.

As shown in Figure 1C, a hydrogen supplying layer 19 for supplying the integrated circuit with hydrogen is formed on the first interlayer insulating film 111 having the first interconnects 14, excluding an area where the capacitor 10 is provided, by plasma CVD. Then, the resultant laminate is annealed at about 450°C for about an hour in an oxygen atmosphere in order to thermally diffuse hydrogen in the hydrogen supplying layer 19. The hydrogen supplying layer 19 is formed of, for example, silicon nitride or silicon nitride oxide and contains a sufficient amount of hydrogen therein.

The annealing is performed in order to allow hydrogen in the hydrogen supplying layer 19 to reach the supporting substrate 1, at a surface of which the integrated circuit 4 is provided, by thermal diffusion. Thus, the integrated circuit 4 recovers from the damage caused by the dry etching which is performed for forming the contact holes 13 during the annealing with oxygen at a temperature of 600°C or higher as is required to form the dielectric film 8. The annealing temperature can be in the range of 300°C to 450°C inclusive. The annealing can be performed in a nitrogen atmosphere, an argon atmosphere or a mixed gas atmosphere of oxygen and

nitrogen and/or argon in lieu of the oxygen atmosphere.

Then, a second interlayer insulating film 151 is formed of an ozone TEOS film on the resultant laminate so as to cover the first interconnects 14. The ozone TEOS film performs self-reflow when being formed, and permits formation of the second interlayer insulating film 151 having no step and a sufficiently flat top surface and thus having satisfactory step coverage although still being sufficiently thin.

The above point will be described with reference to Figures 11A and 11B.

Figure 11A is a schematic cross-sectional view of the second interlayer insulating film 15 formed of silicon oxide (plasma TEOS) on a substrate surface 51 so as to cover wiring patterns 50. The second interlayer insulating film 15 is formed by conventional plasma CVD. Figure 11B is a schematic cross-sectional view of the second interlayer insulating film 151 formed of silicon oxide (ozone TEOS) on the substrate surface 51 so as to cover the wiring patterns 50. The second interlayer insulating film 151 is formed by thermal CVD performed in an atmosphere containing ozone in accordance with the present invention. In the following description, the conventional second interlayer insulating film 15 will also be referred to as the plasma TEOS film, and the second interlayer insulating film 151 according to the present invention will also be referred to as the ozone TEOS film for easier understanding.

By the plasma CVD, solid silicon oxide particles are formed in plasma (gas phase), and the solid silicon oxide particles adhere to the substrate surface 51 and surfaces of the wiring patterns 50. The adhering probability of the solid silicon oxide particles is uniform regardless of the surface to which it adheres. As a result, the resultant plasma TEOS film 15 has substantially the same thickness in areas 52 corresponding to the wiring patterns 50 and an area 53 corresponding to a region between the wiring patterns 50. Accordingly, the plasma TEOS film 15 need to be formed to be relatively thick in order to have a flat top surface.

By the thermal CVD performed in an atmosphere containing ozone, gas-state TEOS as a material gas reacts with oxygen on the substrate surface 51 and the surfaces of the wiring patterns 50. Thus, silicon oxide is produced. The reaction occurs more readily in the area 53 corresponding to the region between the wiring patterns 50 than in the areas 52 corresponding to the wiring patterns 50. Accordingly, the ozone TEOS film 151 is first formed so as to bury the area 53 and then gradually expand to the areas 52 in a self-reflow. In this manner, the ozone TEOS film 151 obtains a flat top surface while remaining relatively thin.

For example, the thickness of the second interlayer insulating film 151 made of ozone TEOS which is required to form the second interconnect 17 thereon without any disconnection is $h_3 =$ about $0.8 \mu\text{m}$ (Figure 1C) on the first interconnect 14 above the upper electrode 9 of the capacitor 10 and $h_4 =$ about $0.5 \mu\text{m}$ (Figure 1C) on the first interlayer insulating film 111 on the edge of the dielec-

tric film 8 formed of a high dielectric constant material film or a ferroelectric material film. As can be understood from this, a sufficient step coverage is achieved while significantly reducing the thickness of the second interlayer insulating film (151), compared to the conventional technology by which the second interlayer insulating film (15) is formed of plasma TEOS.

The ozone used in the above-described process permits, as an active element, the reaction for producing silicon oxide to occur at a lower temperature.

After the formation of the second interlayer insulating film 151, annealing is performed at about 450°C for about an hour in an oxygen atmosphere as a first thermal treatment, thereby allowing the second interlayer insulating film 151 made of an ozone TEOS film to become dense and also supplying the capacitor 10 with oxygen.

Then, as shown in Figure 1D, contact holes 16 are formed so as to run through the second interlayer insulating film 151 and reach the first interconnects 14. A laminate including titanium, aluminum and titanium nitride is formed on the second interlayer insulating film 151 and in the contact holes 16 by sputtering or the like and patterned into a desired pattern. Thus, the second interconnects 17 electrically connected to the first interconnects 14 are formed. Then, annealing is performed at about 400°C for about 30 minutes in a nitrogen atmosphere as a second thermal treatment, thereby making the second interconnects 17 dense and alleviating the stress thereof.

As shown in Figure 1E, a passivation layer 18 is formed of silicon nitride on the resultant laminate by plasma CVD, so as to cover the second interconnects 17. In this manner, the semiconductor device 100 in the first example is completed.

According to the structure of the semiconductor device 100 using ozone TEOS for forming the second interlayer insulating film 151, a sufficient step coverage is obtained. This allows a portion of the second interlayer insulating film 151 located on the capacitor 10 to be thinner. Thus, the stress acting on the capacitor 10 is alleviated.

In the case where the integrated circuit 4 is not damaged while being fabricated, the hydrogen supplying layer 19 can be eliminated. Figure 2 shows a cross-sectional view of a semiconductor device 150 which does not include the hydrogen supplying layer 19. The characteristics of the capacitor 10 are identical with those of the capacitor 10 shown in Figures 1A through 1E.

As described above, the ozone TEOS film 151 is formed by thermal CVD, by which silicon oxide is formed on the substrate by simultaneously supplying TEOS in a gas-state and ozone. This method does not require excitation of plasma upon the film formation.

Figure 3 is a graph illustrating the characteristics (remnant polarization and breakdown voltage) of the capacitor 10 including a dielectric film 8 formed of $\text{SrBi}_2\text{Ta}_2\text{O}_9$, in the case where a second interlayer insulating film 151 formed of ozone TEOS is used, and in the

case where a conventional second interlayer insulating film formed of plasma TEOS is used. For measurement, the plasma TEOS film is first formed to have a thickness of 3.4 μm and then the thickness is reduced to 1.5 μm by resist etch-back. The ozone TEOS film in this example is formed to have a thickness of 1 μm without using etch-back.

A sample including 110 capacitors connected in parallel, each having the above-described structure with an electrode area of 23 μm^2 is produced for the measurement. The remnant polarization of the sample is measured using RT6000A Ferroelectric Tester. The breakdown voltage of the sample is measured using HP4195B.

The following can be seen from Figure 3. In the case where the conventional plasma TEOS film is used, the remnant polarization is 3 $\mu\text{C}/\text{cm}^2$ and the breakdown voltage is 7 V. In the case where the ozone TEOS film in the first example is used, the remnant polarization is 10 $\mu\text{C}/\text{cm}^2$ and the breakdown voltage is 30 V. Thus, the structure according to the first example of the present invention improves the remnant polarization by 7 $\mu\text{C}/\text{cm}^2$ and the breakdown voltage by 23 V, as compared to the conventional structure.

(Example 2)

Figures 4A through 4E are cross-sectional views illustrating a method for fabricating a semiconductor device 200 according to a second example of the present invention. The second example is different from the first example in that, after the second interlayer insulating film 151 is formed, a prescribed part of the

second interlayer insulating film 151 is selectively etched back using the second interconnects 17 as masks.

5 First, the steps shown in Figures 4A through 4C, which are identical with the steps shown in Figures 1A through 1C, are performed.

10 Then, as shown in Figure 4D, contact holes 16 are formed so as to run through the second interlayer insulating film 151 and reach the first interconnects 14. A laminate including titanium, aluminum and titanium nitride is formed on the second interlayer insulating film 151 and in the contact holes 16 by sputtering or the like, and then patterned into a desired pattern. Thus, 15 the second interconnects 17 electrically connected to the first interconnects 14 are formed.

20 The second interlayer insulating film 151 is then etched back using the second interconnects 17 as masks to such an extent as to almost expose the first interconnects 14. Then, annealing is performed at about 400°C for about 30 minutes in a nitrogen atmosphere as a second thermal treatment, thereby making the second interconnects 17 dense and alleviating the stress thereof.

25 As shown in Figure 4E, the passivation layer 18 is formed of silicon nitride on the resultant laminate by plasma CVD, so as to cover the second interconnects 17. In this manner, the semiconductor device 200 in the 30 second example is completed.

Generally, the second interconnects 17 are not provided on an area of the second interlayer insulating

film 151 which is not located on the capacitor 10. According to the structure of the semiconductor device 200 in which the second interlayer insulating film 151 is formed of ozone TEOS and etched back using the second interconnects 17 as masks, the thickness of a part of the second interlayer insulating film 151 located on the capacitor 10 is further reduced, compared to the semiconductor device 100 in the first example. Accordingly, the stress acting on the capacitor 10 is further alleviated.

Figure 5 is a graph illustrating the characteristics (remnant polarization and breakdown voltage) of the capacitor 10 including a dielectric film 8 formed of $\text{SrBi}_2\text{Ta}_2\text{O}_9$, in the case where a second interlayer insulating film 151 formed of ozone TEOS is etched back, and in the case where a second interlayer insulating film 151 formed of ozone TEOS is not etched back. For measurement, the ozone TEOS film is first formed to have a thickness of 1 μm . In the case where the second interlayer insulating film 151 is etched back, the thickness of the film 151 is reduced to 0.5 μm . In the case where the second interlayer insulating film 151 is not etched back, the thickness of the film 151 is maintained 1 μm . The methods and conditions for measuring the remnant polarization and breakdown voltage are the same as those in the first example.

The following can be seen from Figure 5. In the case where the ozone TEOS film is etched back, the remnant polarization is 12 $\mu\text{C}/\text{cm}^2$ (as opposed to 10 $\mu\text{C}/\text{cm}^2$ without etch-back) and the breakdown voltage is 40 V (as opposed to 30 V without etch-back). Thus, the structure according to the second example of the present invention

further improves the remnant polarization by $2 \mu\text{C}/\text{cm}^2$ and the breakdown voltage by 10 V, as compared to the structure according to the first example of the present invention.

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(Example 3)

Figures 6A through 6E are cross-sectional views illustrating a method for fabricating a semiconductor device 300 according to a third example of the present invention.

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The third example is different from the first and second examples in that the second interconnects 17 electrically connected to the first interconnects 14 are also provided on a prescribed area of the second interlayer insulating film 151 which is above the capacitor 10 so as to cover the capacitor 10.

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First, the steps shown in Figures 6A through 6C, which are identical with the steps shown in Figures 1A through 1C, are performed.

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Then, as shown in Figure 6D, contact holes 16 are formed so as to run through the second interlayer insulating film 151 and reach the first interconnects 14. A laminate including titanium, aluminum and titanium nitride is formed on the second interlayer insulating film 151 and in the contact holes 16 by sputtering or the like, and then patterned into a desired pattern. Thus, the second interconnects 17 electrically connected to the first interconnects 14 are formed. The laminate is patterned also to cover the area corresponding to the capacitor 10.

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The second interlayer insulating film 151 may be etched back, using the second interconnects 17 as masks, to such an extent as to almost expose the first interconnects 14. The etch-back on this stage can be eliminated, as seen in Figures 6D and 6E. Then, annealing is performed at about 400°C for about 30 minutes in a nitrogen atmosphere as a second thermal treatment, thereby making the second interconnects 17 dense and alleviating the stress thereof.

Then, as shown in Figure 6E, the passivation layer 18 is formed of silicon nitride on the resultant laminate by plasma CVD, so as to cover the second interconnects 17. In this manner, the semiconductor device 300 in the third example is completed.

According to the structure of the semiconductor device 300 in which the second interconnects 17 are provided on the second interlayer insulating film 151 so as to cover the capacitor 10, the stress applied to the capacitor 10 from the passivation layer 18 is counteracted by the stress generated by the second interconnect 17 located above the capacitor 10. As a result, the stress acting on the capacitor 10 is sufficiently alleviated.

Figure 7 is a graph illustrating the characteristics (remnant polarization and breakdown voltage) of the capacitor 10 including a dielectric film 8 formed of $\text{SrBi}_2\text{Ta}_2\text{O}_9$, in the case where a second interconnect 17 is provided above the capacitor 10, and in the case where a second interconnect 17 is not provided above the capacitor 10. For measurement, the second interlayer insulating film 151 of ozone TEOS film is formed to have a

thickness of 1 μm . The methods and conditions for measuring the remnant polarization and breakdown voltage are the same as those in the first example.

5 The following can be seen from Figure 7. In the case where the second interconnect 17 is provided above the capacitor 10, the remnant polarization is $14 \mu\text{C}/\text{cm}^2$ (as opposed to $10 \mu\text{C}/\text{cm}^2$ without the second interconnect 17 covering the capacitor 10) and the breakdown voltage is 40 V (as opposed to 30 V without the second interconnect 17 covering the capacitor 10). Thus, the structure according to the third example of the present invention further improves the remnant polarization by $4 \mu\text{C}/\text{cm}^2$ and the breakdown voltage by 10 V, as compared to the structure according to the first example of the present invention.

10 In the third example, a second interconnect 17 completely covers the entire capacitor 10. Alternatively, the second interconnect 17 can be formed to cover at least a part of the capacitor 10, whereby the same effect still being obtained. Figure 8A is a plan view of a part of the semiconductor device 300 obtained by the step shown in Figure 6E, the part including the capacitor 10.

20 A second interconnect 17 completely covers the entire capacitor 10 in Figure 8A. Alternatively, the second interconnect 17 can be provided in a substantially zigzag pattern as shown in Figure 8B, or in a mesh pattern as shown in Figure 8C.

25 Two or all of the first through third examples can be combined.

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In the above-described examples, the passivation layer 18 is formed of silicon nitride. Alternatively, a laminate including silicon oxide and silicon nitride can be used, in which case the characteristics of the capacitor 10 are further improved. The laminate including silicon oxide and silicon nitride is formed in the following manner. A silicon oxide film is formed so as to have a tensile stress, and a silicon nitride film generally having a large compressive stress is formed thereon. Thus, the stress applied to the passivation layer 18 is entirely counteracted. Accordingly, the capacitor 10 is not influenced by the stress.

The laminate including silicon oxide and silicon nitride as the passivation layer 18 can be formed by normal-pressure CVD, low-pressure CVD or plasma CVD, using silane gas. The laminate can also be produced by forming a silicon oxide film, which is obtained using ozone TEOS, by normal-pressure CVD or low-pressure CVD and then forming a silicon nitride film thereon by plasma CVD.

Figure 9 is a graph illustrating the characteristics (remnant polarization and breakdown voltage) of the capacitor 10 including a dielectric film 8 formed of $\text{SrBi}_2\text{Ta}_2\text{O}_9$, in the case where a passivation layer 18 is formed of a single layer of silicon nitride, and in the case where a passivation layer 18 is formed of a laminate including silicon oxide and silicon nitride. For measurement, the passivation layer 18 formed of a single layer of silicon nitride is produced to have a thickness of $0.8 \mu\text{m}$ by plasma CVD. The passivation layer 18 formed of a laminate including silicon oxide and silicon nitride

is produced by forming a silicon oxide film having a thickness of 0.1 μm by normal-pressure CVD and then forming a silicon nitride film having a thickness of 0.8 μm thereon by plasma CVD. The methods and conditions for measuring the remnant polarization and breakdown voltage are the same as those in the first example.

The following can be seen from Figure 9. In the case where the passivation layer 18 is formed of a laminate including silicon oxide and silicon nitride, the breakdown voltage is 40 V (as opposed to 30 V). The remnant polarization is the same as in the case where the passivation layer 18 is formed of a single layer of silicon nitride. Thus, the use of a laminate including silicon oxide and silicon nitride as the passivation layer 18 further improves the breakdown voltage by 10 V, as compared to the structure according to the first example of the present invention.

The passivation layer 18 formed of a laminate including silicon oxide and silicon nitride can be combined with any structure described in the first through third examples.

In the first through third examples, the first interlayer insulating film 111 is formed of an ozone TEOS film. Alternatively, the first interlayer insulating film 111 can be formed of a silicon oxide film produced by normal-pressure CVD or low-pressure CVD using silane or disilane, or a silicon oxide film produced in this manner and further treated by phosphorus doping.

In the first through third examples, the first interconnect 14 is formed of a laminate including titanium, titanium nitride, aluminum and titanium nitride. Alternatively, the first interconnect 14 can be formed of a laminate including titanium, titanium nitride and aluminum; a laminate including titanium, titanium tungsten, aluminum and titanium tungsten; or a laminate including titanium, titanium tungsten and aluminum.

The ozone TEOS film forming the second interlayer insulating film 151 preferably has a Si-OH bond absorption coefficient of 800 cm^{-1} or less at a wavelength corresponding to 3450 cm^{-1} . When the moisture content in the ozone TEOS film is thus reduced as low as possible, moisture which deteriorates the characteristics of the capacitor 10, especially OH radicals and H radicals, is restricted from entering the capacitor 10. Thus, generation of cracks by thermal treatment after the film formation is suppressed. Accordingly, the characteristics of the capacitor 10 are further improved.

The ozone TEOS film forming the second interlayer insulating film 151 preferably has a tensile stress of $1 \times 10^7\text{ dyn/cm}^2$ to $3 \times 10^9\text{ dyn/cm}^2$ inclusive. Due to such a tensile stress, adverse effects on the capacitor (e.g., undesirable restriction of polarization) caused by the stress applied to the capacitor are alleviated. Thus, the characteristics of the capacitor 10 are improved. A stress outside the above-mentioned range tends to cause the characteristics of the capacitor 10 to be deteriorated.

This effect largely relies on the fact that the stress is a tensile stress. A capacitor which is supplied with a tensile stress, e.g., from an ozone TEOS film has more preferable characteristics than a capacitor which is supplied with a compressive stress, e.g., from a plasma TEOS film, even when the absolute values of the stresses are equal.

The ozone TEOS film has a tensile stress presumably for the following reason. Upon the film formation, TEOS gas and ozone reacts on the substrate surface to form silicon oxide while a volume is reduced. In other words, a volume of the resultant silicon oxide (i.e., the resultant ozone TEOS film) becomes smaller than the sum of volumes of the involved TEOS gas and ozone. Furthermore, the subsequent thermal treatment causes the resultant ozone TEOS film to become more dense, thereby further constricting the film. Thus, the ozone TEOS film has a tensile stress, and accordingly, a tensile stress acts on the dielectric film 8 of the capacitor 10 provided below the ozone TEOS film.

On the other hand, a plasma TEOS film has a compressive stress presumably for the following reason. In this case, silicon oxide in the form of solid particles formed in the gas phase are deposited, and thus, a volume reduction does not occur. Furthermore, the solid silicon oxide particles tend to densely deposit, and further expand. Accordingly, a plasma TEOS film has a compressive stress. It is presumed that, when the compressive stress acts on the dielectric film 8 of the capacitor 10, generation of polarization in a direction connecting the upper electrode 9 and the lower electrode 7 (i.e., a

direction perpendicular to the substrate) is restricted, as a result of which the characteristics of the capacitor 10 are deteriorated.

5 The thickness of the ozone TEOS film forming the second interlayer insulating film 151 is preferably between 0.3 μm to 1 μm inclusive. When the thickness exceeds 1 μm , the stress of the ozone TEOS film increases. The increased thickness may disadvantageously
10 deteriorates the characteristics of the capacitor 10, and also tends to generate cracks when the first thermal treatment is performed as a part of post-treatment. When the thickness of the ozone TEOS film is less than 0.3 μm , sufficient step coverage is not obtained, and treatment
15 of the ozone TEOS film may disadvantageously generate etching residues.

 The ozone concentration upon forming the ozone TEOS film as the second interlayer insulating film 151 is preferably 5.5% or more. When the ozone concentration is set to such a range, the stress included in the ozone
20 TEOS film is alleviated, and generation of cracks by thermal treatment is restricted. Accordingly, the characteristics of the capacitor 10 are further improved.

25 In the first to third examples, the temperature for the first thermal treatment is 450°C. The temperature can be in the range of 300°C to 450°C inclusive. When the temperature is in this range, the silicon oxide
30 film produced using ozone TEOS becomes dense. Thus, the characteristics of the capacitor 10 are further improved. Furthermore, the first thermal treatment can be performed in a mixed gas atmosphere of oxygen and another gas in

lieu of the oxygen atmosphere. When the mixed gas atmosphere is used, oxygen is supplied to the dielectric film 8, and thus, the characteristics of the capacitor 10 are further improved.

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After the first thermal treatment, it is preferable that the ozone TEOS film forming the second interlayer insulating film 151 has a tensile stress of 1×10^7 dyn/cm² to 2×10^9 dyn/cm² inclusive. When the stress in the ozone TEOS film (second interlayer insulating film 151) is in the above-mentioned range even after the volume reduction of the ozone TEOS film (second interlayer insulating film 151) occurs due to the thermal treatment, the stress acting on the capacitor 10 is alleviated and thus deterioration in the characteristics of the capacitor 10 is restricted.

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In the first through third examples, the second interconnect 17 is formed of a laminate including titanium, aluminum and titanium nitride. Alternatively, second interconnect 17 can be formed of a laminate including titanium and aluminum or a laminate including titanium, aluminum, titanium tungsten. The same effects are obtained.

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In the first through third examples, the temperature for the second thermal treatment is 400°C. The temperature can be in the range of 300°C to 450°C inclusive. When the temperature is in this range, the stress of the second interconnect 17 is alleviated while the second interconnect 17 becomes dense. The second thermal treatment can be performed in an argon atmosphere, a helium atmosphere, or a mixed gas atmosphere of nitrogen

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and these gases in lieu of the nitrogen atmosphere. The same effects of obtaining the dense second interconnect 17 and alleviating the stress thereof are obtained.

5 As described above, according to the present invention, the stress acting on the capacitor is alleviated. Furthermore, since the stress is a tensile stress, the deterioration in the characteristics of the capacitor caused by the stress is restricted, and thus the capacitor obtains satisfactory characteristics. A semiconductor including such a capacitor enjoys excellent reliability even when having a multiple-interconnect structure.

10 Various other modifications will be apparent to and can be readily made by those skilled in the art without departing from the scope and spirit of this invention. Accordingly, it is not intended that the scope of the claims appended hereto be limited to the description as set forth herein, but rather that the claims be broadly construed.

WHAT IS CLAIMED IS:

1. A semiconductor device, comprising:

a capacitor provided on a supporting substrate having an integrated circuit thereon and including a lower electrode, a dielectric film, and an upper electrode;

a first interlayer insulating film provided so as to cover the capacitor;

a first interconnect selectively provided on the first interlayer insulating film and electrically connected to the integrated circuit and the capacitor through a first contact hole formed in the first interlayer insulating film;

a second interlayer insulating film formed of ozone TEOS and provided so as to cover the first interconnect;

a second interconnect selectively provided on the second interlayer insulating film and electrically connected to the first interconnect through a second contact hole formed in the second interlayer insulating film; and

a passivation layer provided so as to cover the second interconnect.

2. A semiconductor device according to claim 1, wherein the dielectric film is formed from either a dielectric material having a high dielectric constant or a ferroelectric material.

3. A semiconductor device according to claim 1, wherein the second interconnect is provided on the second interlayer insulating film so as to cover at least a part of

the capacitor.

4. A semiconductor device according to claim 1, wherein the passivation layer is formed from a laminate including a silicon oxide film and a silicon nitride film.

5. A semiconductor device according to claim 1, further comprising a hydrogen supplying layer provided between the first interconnect and the second interlayer insulating film excluding an area in which the capacitor is provided.

6. A semiconductor device according to claim 1, wherein the first interconnect is formed from a laminate including titanium, titanium nitride, aluminum and titanium nitride; a laminate including titanium, titanium nitride and aluminum; a laminate including titanium, titanium tungsten, aluminum and titanium tungsten; or a laminate including titanium, titanium tungsten and aluminum.

7. A semiconductor device according to claim 1, wherein a Si-OH bond absorption coefficient of the second interlayer insulating film at a wavelength corresponding to 3450 cm^{-1} is 800 cm^{-1} or less.

8. A semiconductor device according to claim 1, wherein the second interlayer insulating film has a tensile stress of $1 \times 10^7\text{ dyn/cm}^2$ to $3 \times 10^9\text{ dyn/cm}^2$ inclusive.

9. A semiconductor device according to claim 1, wherein the second interlayer insulating film has a thickness of $0.3\text{ }\mu\text{m}$ to $1\text{ }\mu\text{m}$ inclusive.

10. A semiconductor device according to claim 1, wherein the second interconnect is formed from a laminate including titanium, aluminum and titanium nitride; a laminate including titanium and aluminum; or a laminate including titanium, aluminum and titanium tungsten.

11. A method for fabricating a semiconductor device, comprising the steps of:

sequentially forming a lower electrode, a dielectric film, and an upper electrode on a supporting substrate having an integrated circuit, thereby forming a capacitor;

forming a first interlayer insulating film so as to cover the capacitor;

forming a first contact hole in the first interlayer insulating film;

selectively forming a first interconnect in the first contact hole and on a prescribed area of the first interlayer insulating film so as to be electrically connected to the integrated circuit and the capacitor;

forming a second interlayer insulating film of ozone TEOS so as to cover the first interconnect;

subjecting the second interconnect to a first thermal treatment;

forming a second contact hole in the second interlayer insulating film;

selectively forming a second interconnect in the second contact hole and on a prescribed area of the second interlayer insulating film so as to be electrically connected to the first interconnect;

subjecting the second interconnect to a second thermal treatment; and

forming a passivation layer so as to cover the

second interconnect.

12. A method for fabricating a semiconductor device according to claim 11, wherein the dielectric film is formed from either a dielectric material having a high dielectric constant or a ferroelectric material.

13. A method for fabricating a semiconductor device according to claim 11, further comprising the step of etching back the second interlayer insulating film using the second interconnect as a mask to such an extent as to almost expose the first interconnect.

14. A method for fabricating a semiconductor device according to claim 11, wherein the step of forming the second interconnect includes the step of forming the second interconnect so as to cover at least a part of the capacitor.

15. A method for fabricating a semiconductor device according to claim 11, wherein:

the passivation layer is formed of a laminate including a silicon oxide film and a silicon nitride film, and

the silicon oxide film is formed by normal-pressure CVD, low-pressure CVD or plasma CVD, with using silane, disilane or ozone TEOS, so as to have a tensile stress.

16. A method for fabricating a semiconductor device according to claim 11, further comprising the steps of:

after the first interconnect is formed, forming a hydrogen supplying layer on the first interconnect

excluding an area where the capacitor is provided; and
performing a third thermal treatment.

17. A method for fabricating a semiconductor device according to claim 16, wherein the hydrogen supplying layer is formed from either silicon nitride or silicon nitride oxide by plasma CVD.

18. A method for fabricating a semiconductor device according to claim 16, wherein the third treatment performed after the formation of hydrogen supplying layer is performed at a temperature in the range of 300°C to 450°C inclusive.

19. A method for fabricating a semiconductor device according to claim 16, wherein the third treatment performed after the formation of the hydrogen supplying layer is performed in an oxygen atmosphere, a nitrogen atmosphere, an argon atmosphere or an atmosphere of a mixed gas thereof.

20. A method for fabricating a semiconductor device according to claim 11, wherein the first interlayer insulating film is formed of silicon oxide by normal-pressure CVD or low-pressure CVD, with using silane, disilane or ozone TEOS.

21. A method for fabricating a semiconductor device according to claim 11, wherein the first interlayer insulating film is formed of phosphorus-doped silicon oxide by normal-pressure CVD or low-pressure CVD.

22. A method for fabricating a semiconductor device according to claim 11, wherein an ozone concentration upon forming the second interlayer insulating film using ozone TEOS is set to be at 5.5% or more.

23. A method for fabricating a semiconductor device according to claim 11, wherein the second interlayer insulating film after being subjected with the first thermal treatment has a tensile stress of 1×10^7 dyn/cm² to 2×10^9 dyn/cm² inclusive.

24. A method for fabricating a semiconductor device according to claim 11, wherein the first thermal treatment is performed at a temperature in the range of 300°C to 450°C inclusive.

25. A method for fabricating a semiconductor device according to claim 11, wherein the first thermal treatment is performed in an atmosphere containing at least oxygen.

26. A method for fabricating a semiconductor device according to claim 11, wherein the second thermal treatment is performed at a temperature in the range of 300°C to 450°C inclusive.

27. A method for fabricating a semiconductor device according to claim 11, wherein the second thermal treatment is performed in an atmosphere containing at least one of nitrogen, argon and helium.

ABSTRACT OF THE DISCLOSURE

A semiconductor device includes: a capacitor provided on a supporting substrate having an integrated circuit thereon and including a lower electrode, a dielectric film, and an upper electrode; a first interlayer insulating film provided so as to cover the capacitor; a first interconnect selectively provided on the first interlayer insulating film and electrically connected to the integrated circuit and the capacitor through a first contact hole formed in the first interlayer insulating film; a second interlayer insulating film formed of ozone TEOS and provided so as to cover the first interconnect; a second interconnect selectively provided on the second interlayer insulating film and electrically connected to the first interconnect through a second contact hole formed in the second interlayer insulating film; and a passivation layer provided so as to cover the second interconnect.

FIG. 1A

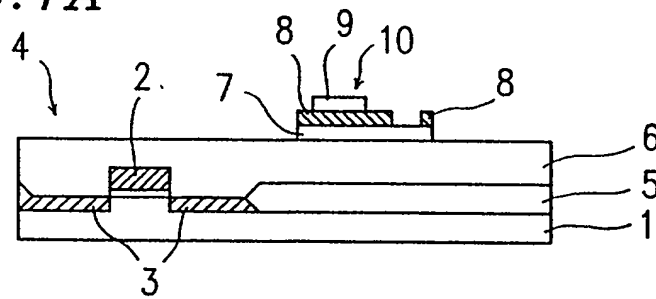


FIG. 1B

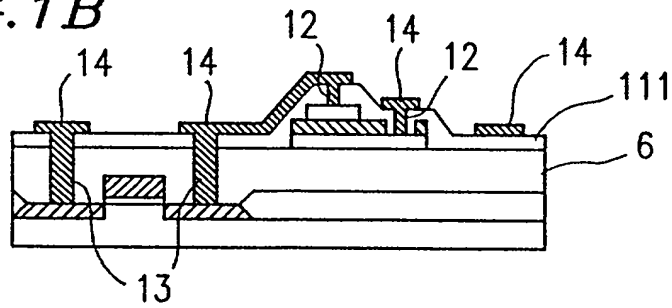


FIG. 1C

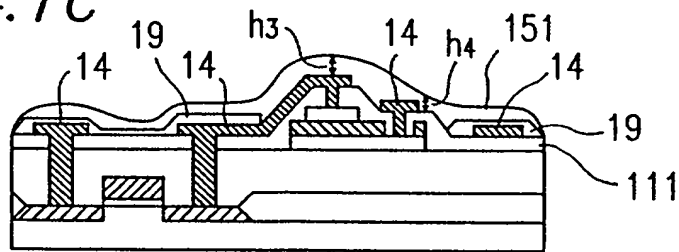


FIG. 1D

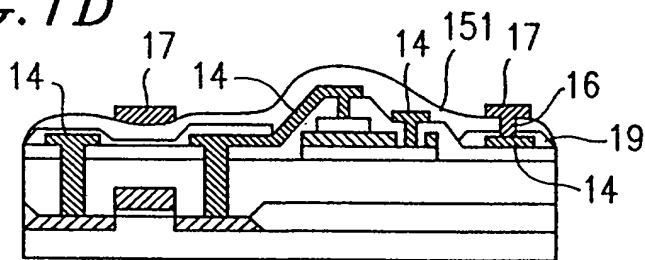
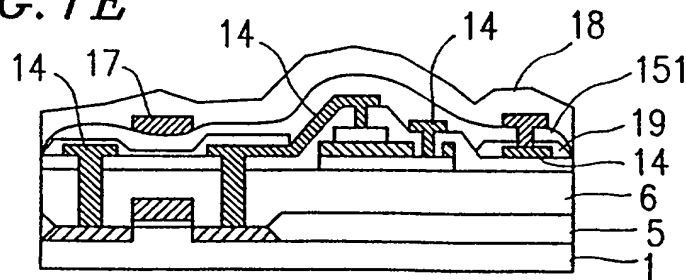


FIG. 1E



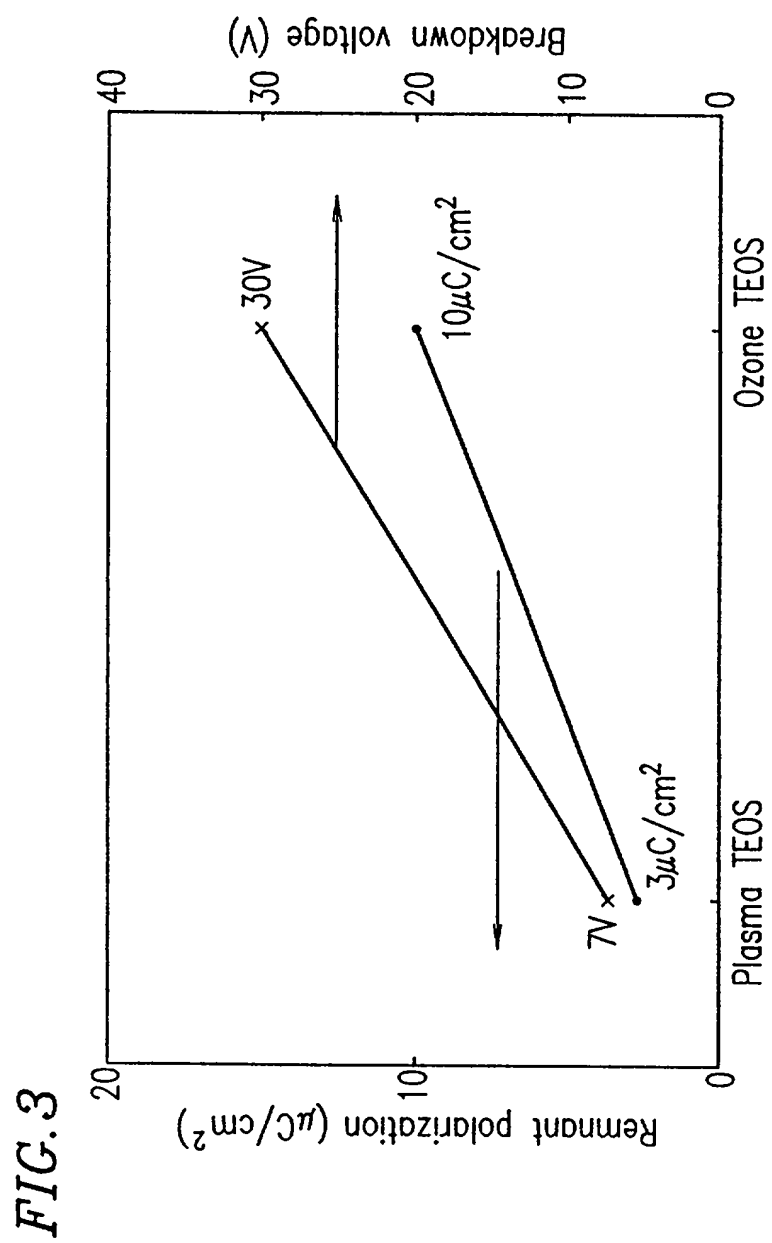


FIG. 4A

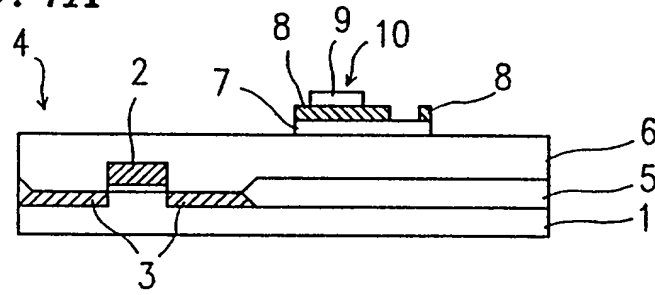


FIG. 4B

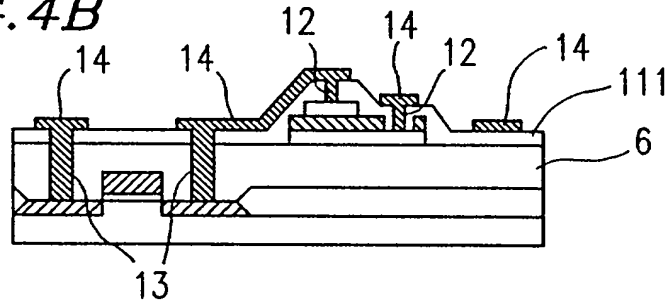


FIG. 4C

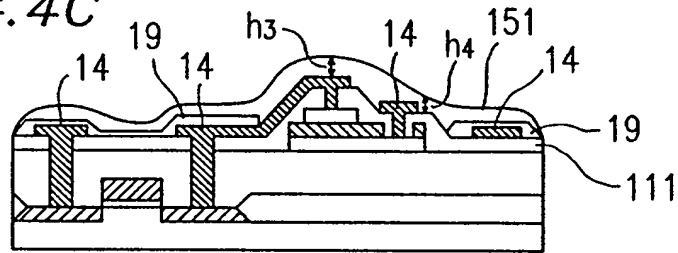


FIG. 4D

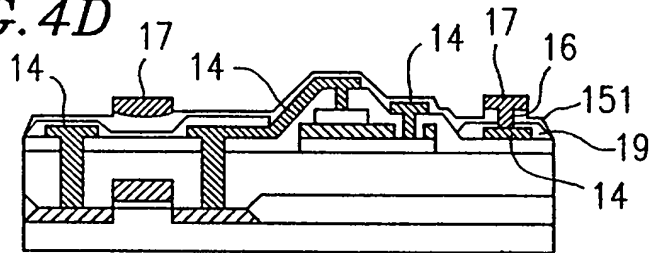
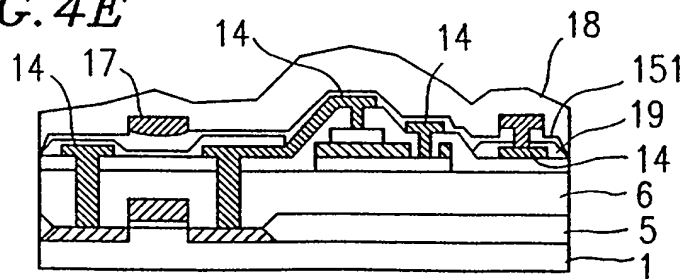


FIG. 4E



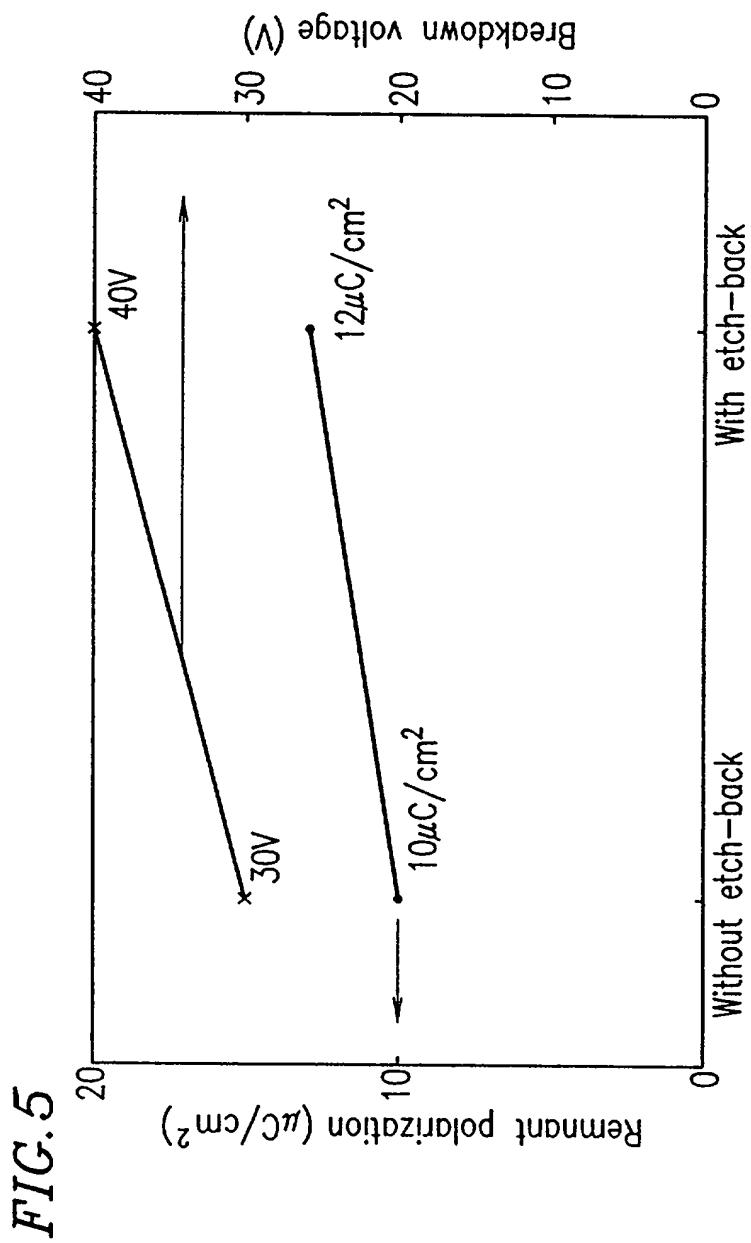
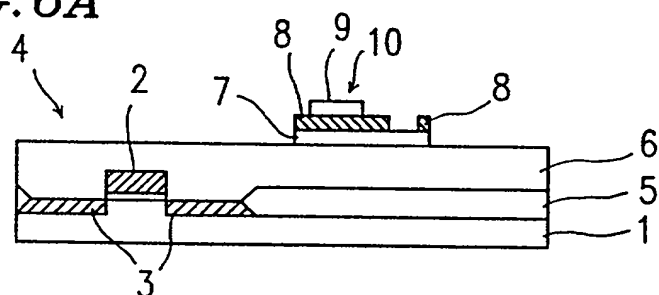
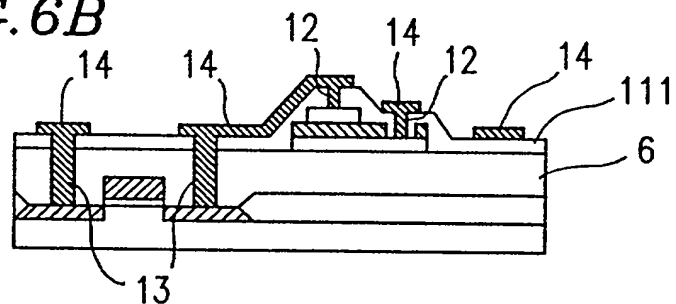
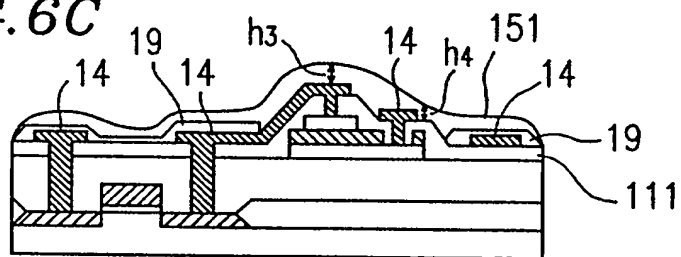
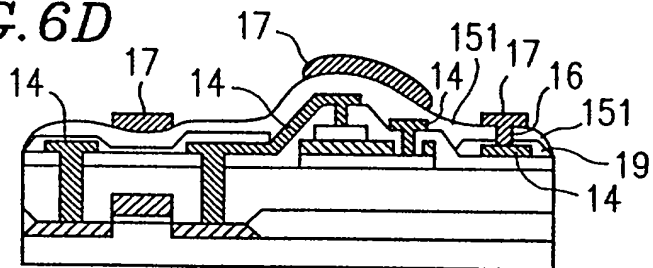
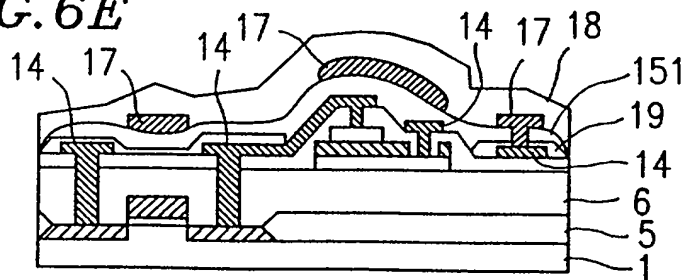


FIG. 6A*FIG. 6B**FIG. 6C**FIG. 6D**FIG. 6E*

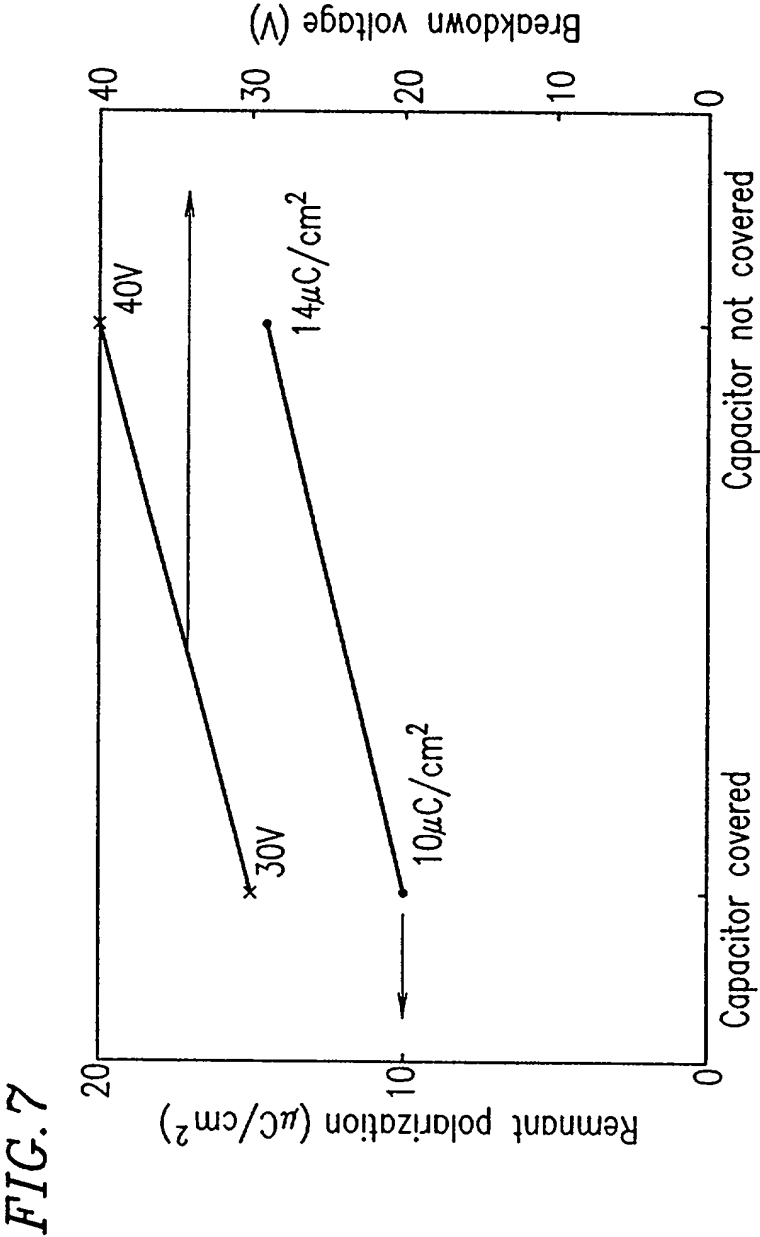
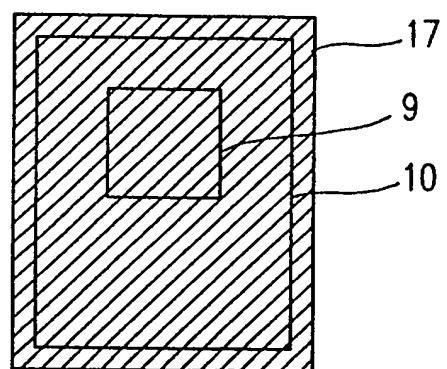
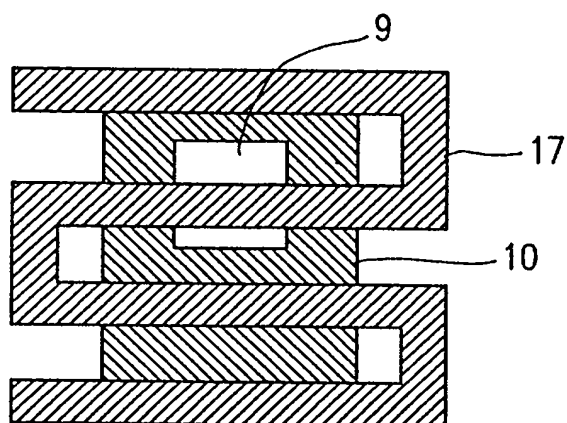
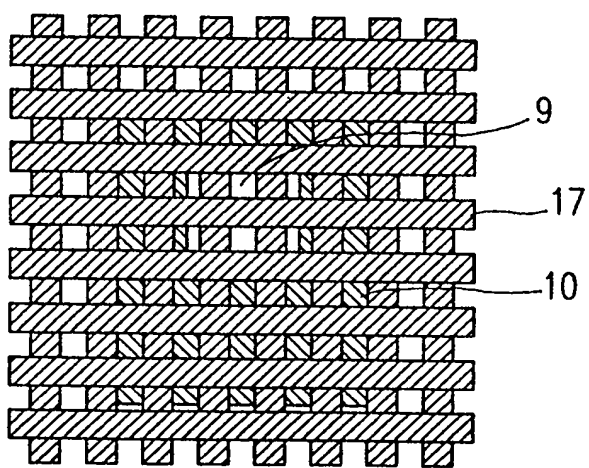


FIG. 7 is a graph showing Breakdown voltage (V) vs. Remnant polarization ($\mu\text{C}/\text{cm}^2$) for capacitor covered and not covered conditions.

FIG. 8A*FIG. 8B**FIG. 8C*

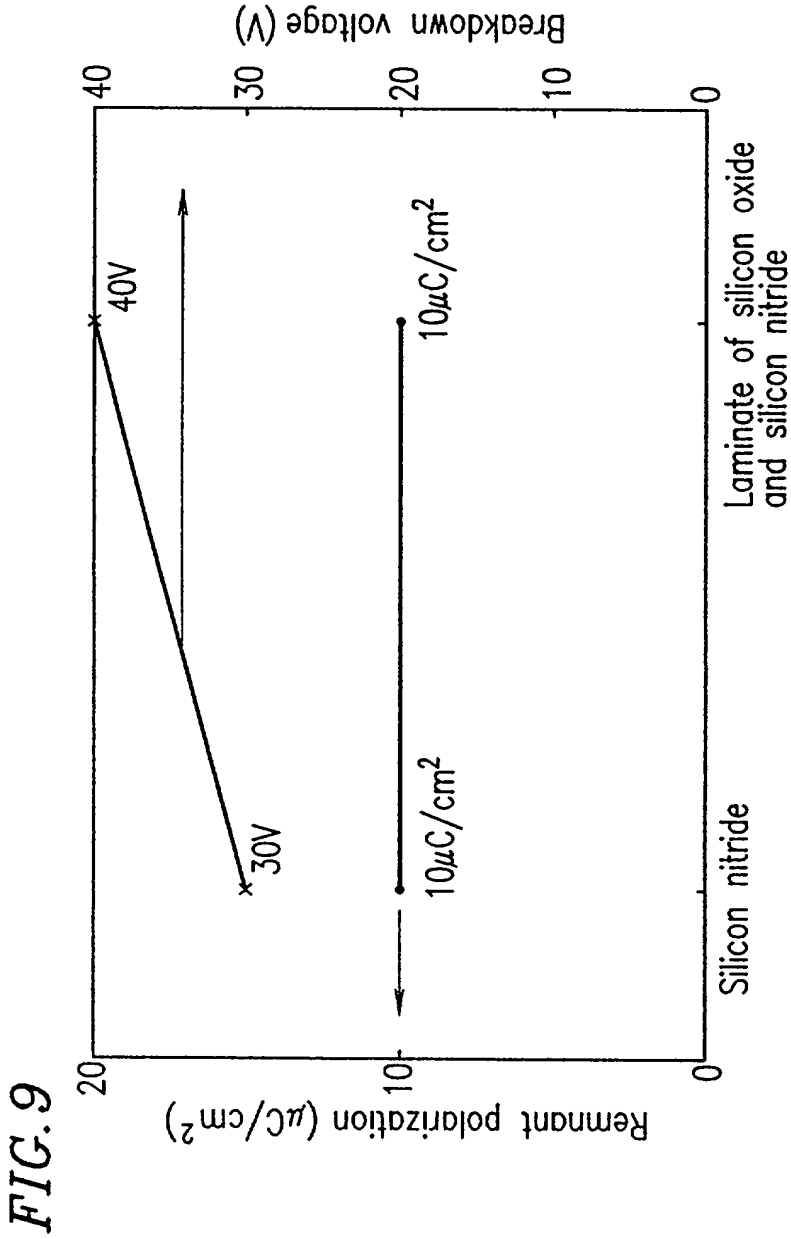


FIG. 10A

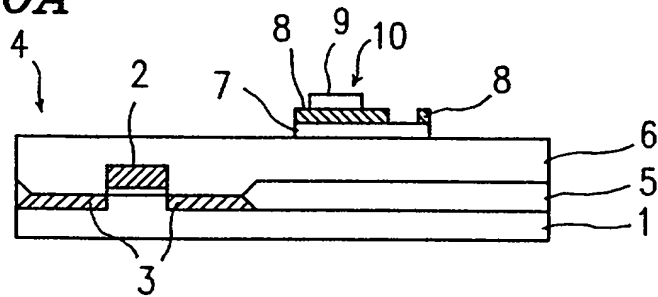


FIG. 10B

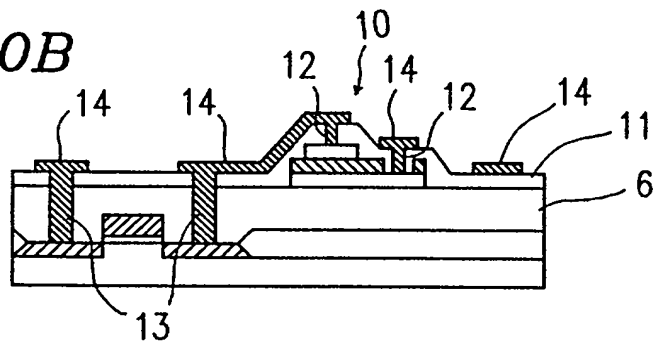


FIG. 10C

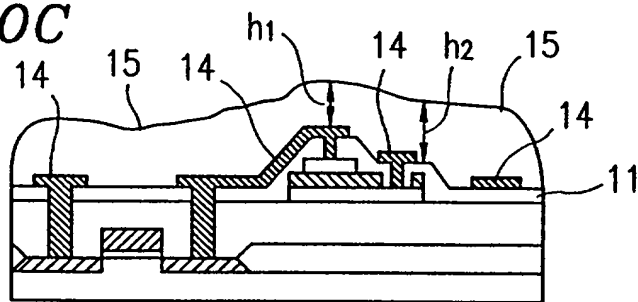


FIG. 10D

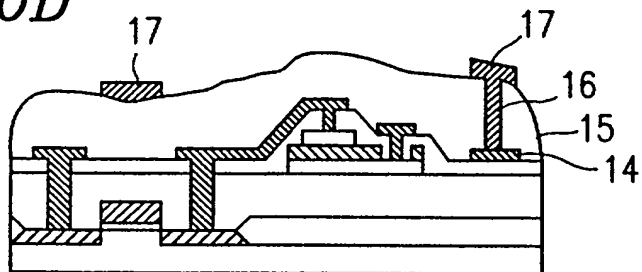


FIG. 10E

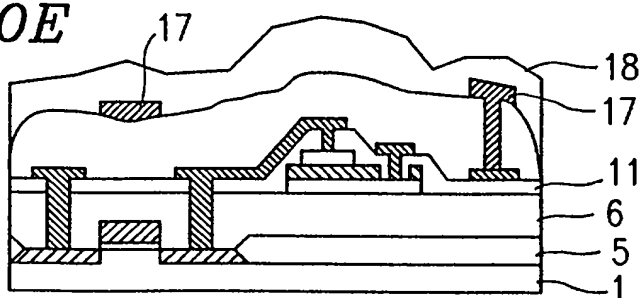


FIG. 11A

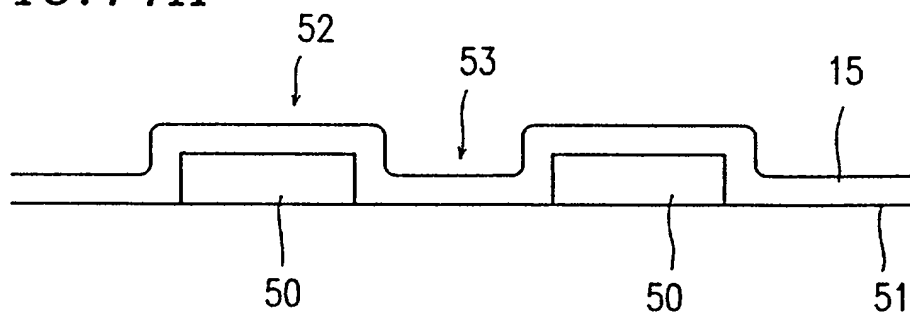
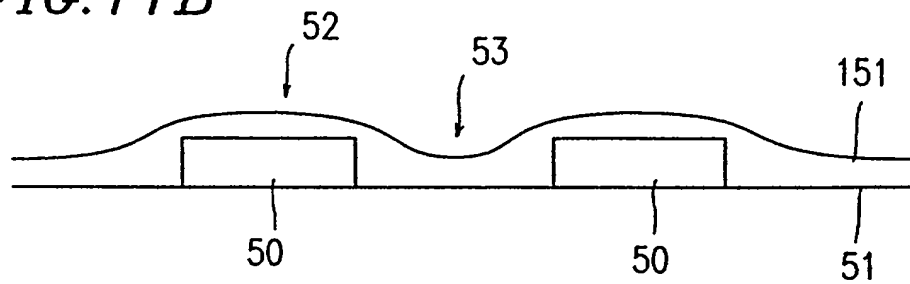


FIG. 11B



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Yoshihisa Nagano et al. : Art Unit:
Serial No.: To Be Assigned : Examiner:
Filed: June 24, 1998 :
FOR: SEMICONDUCTOR DEVICE AND :
METHOD FOR FABRICATING THE SAME

ASSOCIATE POWER OF ATTORNEY

Assistant Commissioner for Patents
Washington, D.C. 20231

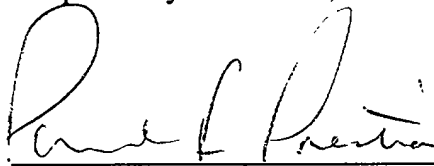
S I R :

Please recognize as associate attorneys for the above-identified patent application Paul F. Prestia, Registration No. 23,031; Allan Ratner, Registration No. 19,717; Andrew L. Ney, Registration No. 20,300; Kenneth N. Nigon, Registration No. 31,549; Kevin R. Casey, Registration No. 32,117; Benjamin E. Leace, Registration No. 33,412; Lawrence E. Ashery, Registration No. 34,515; James C. Simmons, Registration No. 24,842; Robert L. Andersen, Registration No. 25,771; Christopher R. Lewis, Registration No. 36,201; Louis W. Beardell, Jr., Registration No. 40,506; Rocco L. Adornato, Registration No. 40,480; Jacques L. Etkowicz, Registration No. 41,738; Eric L. Dichter, Registration No. 41,708; Mark J. Marcelli, Registration No. 36,593; Christopher J. Dervishian, Registration No. 42,480; Joshua L. Cohen, Registration No. 38,040; and Jack J. Jankovitz, Registration No. P42,690, all of Ratner & Prestia, attorneys at law, to prosecute this application, and to transact all business in the U. S. Patent and Trademark Office in connection therewith.

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The Assistant Commissioner for Patents is
hereby authorized to charge payment to
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Date of Deposit: June 24, 1998

I hereby certify that this paper and fee are being deposited, under 37 C.F.R. § 1.10 and with sufficient postage, using the "Express Mail Post Office to Addressee" service of the United States Postal Service on the date indicated above and that the deposit is addressed to the Assistant Commissioner for Patents, Washington, D.C. 20231.


Jan Landis

P15260

SEMICONDUCTOR DEVICE AND
METHOD FOR FABRICATING THE SAME

Declaration and Power of Attorney For Patent Application

English Language Declaration

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name,

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

SEMICONDUCTOR DEVICE AND METHOD FOR FABRICATING THE SAME
the specification of which is attached hereto unless the following box is checked:

☐ was filed on _____ as
United States Application Number or PCT International Application Number _____
and was amended on _____ (if applicable).

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR § 1.56.

I hereby claim foreign priority benefits under 35 U.S.C. § 119(a)-(d) or § 365(b) of any foreign application(s) for patent or inventor's certificate, or § 365(a) of any PCT International application which designated at least one country other than the United States, listed below and have also identified below by checking the box, any foreign application for patent or inventor's certificate, or PCT International application having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s)			Priority Not Claimed
<u>9-166991</u>	<u>Japan</u>	<u>24/06/1997</u>	<input type="checkbox"/>
(Number)	(Country)	(Day/Month/Year Filed)	
_____	_____	_____	<input type="checkbox"/>
(Number)	(Country)	(Day/Month/Year Filed)	

I hereby claim the benefit under 35 U.S.C. § 119(e) of any United States provisional application(s) listed below.

_____	_____
(Application Number)	(Filing Date)
_____	_____
(Application Number)	(Filing Date)

I hereby claim the benefit under 35 U.S.C. § 120 of any United States application(s), or 365(c) of any PCT International application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of 35 U.S.C. § 112, I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR § 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application:

(Application Number)

(Filing Date)

(Status - patented, pending, abandoned)

(Application Number)

(Filing Date)

(Status - patented, pending, abandoned)

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Kenneth N. Nigon	Reg.No. 31,549	Louis W. Beardell, Jr.	Reg.No. 40,506		
Kevin R. Casey	Reg.No. 32,117	Ian M. Hughes	Reg.No. 41,083		
Benjamin E. Leace	Reg.No. 33,412	Rocco L. Adornato	Reg.No. 40,480		
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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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Sixth inventor's signature _____ Date _____

Residence _____

Citizenship _____

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Seventh inventor's signature _____ Date _____

Residence _____

Citizenship _____

Post Office Address _____